a gate electrode provided on the surface of the first electron supply layer exposed from a bottom of the narrow recess opening; and

a source electrode and a drain electrode provided on the second contact layer outside the wide recess opening so that the wide recess opening is sandwiched between the source electrode and the drain electrode.

5. The heterojunction type compound semiconductor field effect transistor according to claim 4, wherein each of the electric field strength reducing layer and the recess stopper layer is thinner than the first contact layer.

6. The heterojunction type compound semiconductor field effect transistor according to claim 4, wherein the compound semiconductor substrate includes a semi-insulating GaAs substrate, a buffer layer provided on the semi-insulating GaAs substrate and having a superlattice structure, and a second electron supply layer provided on the buffer layer and under the channel layer and composed of AlGaAs doped with n type impurities.

7. A heterojunction type compound semiconductor field effect transistor comprising:

a channel layer provided on a compound semiconductor substrate and composed of intrinsic GaAs or InGaAs;

a first electron supply layer provided on the channel layer and composed of AlGaAs doped with n type impurities;

an electric field strength reducing layer provided on the first electron supply layer and composed of intrinsic InGaP;

a first contact layer provided on the electric field strength reducing layer and composed of GaAs or InGaAs doped with n type impurities;

a recess stopper layer provided on the first contact layer and composed of intrinsic InGaP;

a second contact layer provided on the recess stopper layer and composed of GaAs doped with n type impurities of a concentration higher than that of the first contact layer;

a wide recess opening formed to penetrate the second contact layer so as to expose a surface of the recess stopper layer;

a narrow recess opening formed in the wide recess opening to penetrate the recess stopper layer and the first contact layer so as to expose a surface of the electric field strength reducing layer;

a gate electrode provided on the surface of the electric field strength reducing layer exposed from a bottom of the narrow recess opening; and

a source electrode and a drain electrode provided on the second contact layer outside the wide recess opening so that the wide recess opening is sandwiched between the source electrode and the drain electrode.

8. The heterojunction type compound semiconductor field effect transistor according to claim 7, wherein each of the electric field strength reducing layer and the recess stopper layer is thinner than the first contact layer.

9. The heterojunction type compound semiconductor field effect transistor according to claim 7, wherein the compound semiconductor substrate includes a semi-insulating GaAs substrate, a buffer layer provided on the semi-insulating GaAs substrate and having a superlattice structure, and a second electron supply layer provided on the buffer layer and under the channel layer and composed of AlGaAs doped with n type impurities.

10. A heterojunction type compound semiconductor field effect transistor comprising:

a channel layer provided on a compound semiconductor substrate and composed of intrinsic GaAs or InGaAs;

a first electron supply layer provided on the channel layer and composed of AlGaAs doped with n type impurities;

an electric field strength reducing layer provided on the first electron supply layer and composed of intrinsic InGaP;

a first contact layer provided on the electric field strength reducing layer and composed of GaAs or InGaAs doped with n type impurities;

a recess stopper layer provided on the first contact layer and composed of intrinsic InGaP;

a second contact layer provided on the recess stopper layer and composed of GaAs doped with n type impurities of a concentration higher than that of the first contact layer;

a wide recess opening formed to penetrate the second contact layer and the recess stopper layer so as to expose a surface of the first contact layer;

a narrow recess opening formed in the wide recess opening to penetrate the first contact layer so as to expose a surface of the electric field strength reducing layer;

a gate electrode provided on the surface of the electric field strength reducing layer exposed from a bottom of the narrow recess opening; and

a source electrode and a drain electrode provided on the second contact layer outside the wide recess opening so that the wide recess opening is sandwiched between the source electrode and the drain electrode.

11. The heterojunction type compound semiconductor field effect transistor according to claim 10, wherein each of the electric field strength reducing layer and the recess stopper layer is thinner than the first contact layer.

12. The heterojunction type compound semiconductor field effect transistor according to claim 10, wherein the compound semiconductor substrate includes a semi-insulating GaAs substrate, a buffer layer provided on the semi-insulating GaAs substrate and having a superlattice structure, and a second electron supply layer provided on the buffer layer and under the channel layer and composed of AlGaAs doped with n type impurities.

13. A manufacturing method for a heterojunction type compound semiconductor field effect transistor, the method comprising:

forming a channel layer composed of intrinsic GaAs or InGaAs on a compound semiconductor substrate;

forming a first electron supply layer composed of AlGaAs on the channel layer;

forming an electric field strength reducing layer composed of intrinsic InGaP on the electron supply layer;